35 U.S.C. § 102 & 103

The Office Action rejected claims 2-3 and 6-8 under 35 U.S.C. § 102 over Teo. Applicants traverse those rejections for at least the following reasons.

Claim 2

Claim 2 has been amended to be in independent form, and to clarify that the "critical dimension" of the conductive line in claim 2 is its **width**, as it is defined in the Specification (see FIGs. 4A, 5A, and 10 and page 11, lines 12-15; see also page 6, lines 27-28; page 7, lines 14-17; page 8, lines 26-31; page 10, line 33- page 11, line 5), not its thickness.

Among other things, the method of claim 2 includes forming a patterned photosensitive film on the second interlayer dielectric layer, the patterned photosensitive film *defining an opening therein having a width that is greater than a width of the conductive line*. No such feature is disclosed by Teo.

The Office Action states that Teo discloses forming a pattern photosensitive film 17 defining an opening (18???) therein having a width that is greater than the critical dimension (i.e., thickness) of the conductive line 13.

Applicants respectfully disagree.

At the outset, as explained above, the "critical dimension" of the conductive line in claim 2 is its width (see FIGs. 4A, 5A, and 10 and page 11, lines 12-15; see also page 6, lines 27-28; page 7, lines 14-17; page 8, lines 26-31; page 10, line 33- page 11, line 5). Meanwhile, there is no suggestion in either the Specification or in Teo that the "thickness" of a conductive line is a critical dimension. So Applicants

cannot understand the basis for such a statement in the Office Action that the "thickness" of the conductive line 13 is the "critical dimension." In addition to being inconsistent with the definition of "the critical dimension" provided by Applicants in the Specification and Drawings, Applicants do not understand what is supposed to be "critical" about this dimension? In any event, the Applicants have amended claim 2 to recite that the critical dimension in claim 2 is the width of the conductive line.

Clearly, from inspection of FIGs. 3-8 of Teo, the opening 18 does ***not*** have a width that is greater than the width of the conductive line 13. So it is not possible for Teo to anticipate the method of claim 2.

For at least these reasons, Applicant respectfully submits that claim 2 is patentable over Teo.

Claims 3, 6, and 7

Claims 3, 6, and 7, dependent from claim 2, are deemed allowable for similar reasons to those set forth above with respect to claim 2.

Claims 4-5

Claims 4 and 5 depend from claim 2.

The Office Action rejected claims 4-5 under 35 U.S.C. § 102 over Teo in view of Kusumi. Applicant respectfully submits that the addition of Kusumi fails to remedy the shortcomings of Teo discussed above with respect to claim 2.

Accordingly, Applicants respectfully submit that claims 4-5 are patentable over Teo in view of Kusumi.

Claim 8

Claim 8 has been amended to be in independent form without any other changes, and accordingly claim 8 has exactly the same scope as it did prior to this amendment.

Among other things, in the method of claim 8, forming the conductive line comprises forming a dielectric film pattern defining a line-shaped opening on the first interlayer dielectric layer, and depositing conductive material in the line-shaped opening. No such feature is disclosed by Teo.

The Office Action states that Teo discloses forming a dielectric film pattern defining a line-shaped opening 18 on the first interlayer dielectric layer 12, and depositing conductive material 19 in the line-shaped opening 18.

However, this is not what claim 8 recites..

Applicants note that claim 8 does not merely recite "forming a dielectric film pattern defining a line-shaped opening on the first interlayer dielectric layer, and depositing conductive material in the line-shaped opening." Instead, claim 8 recites "forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer" and that "*forming the conductive line* comprises forming a dielectric film pattern defining a line-shaped opening on the first interlayer dielectric layer, and depositing conductive material in the line-shaped opening."

Thus, the conductive line that claim 8 states is formed by forming a dielectric film pattern defining a line-shaped opening on the first interlayer dielectric layer, and depositing conductive material in the line-shaped opening in the line-shaped opening,

is and must be *the very same conductive line* that is formed on the first interlayer dielectric layer and which is to be connected to the conductive region In the rejection of claim 1 (from which claim 8 depended) the Office Action stated that this conductive line allegedly corresponds to element 13 of Teo. However, in claim 8, the Office Action states that the conductive material is 19, which does not form the conductive line 13.

Moreover, the Office Action fails to identify anything in Teo allegedly corresponding to the "dielectric film pattern" that defines the "line-shaped opening" (allegedly, element 18).

Finally, the Office Action has not cited anything in Teo that suggests that the opening 18 is line-shaped. Indeed, Teo teaches that the opening 18 is a "hole" (see col. 3, lines 23-35). In contrast, the opening of claim 8 is "line-shaped" so as to provide an opening for forming a conductive ***line*** (e.g., element 34 in FIGs. 4B and 5B; see also page 6, lines 10-16).

For at least these reasons, Applicant respectfully submits that claim 8 is patentable over Teo.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 2-10, 14, 15 and 21-23, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to

contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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Date: 19 February 2003

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Version with Markings to Show Changes Made

In the Claims:

Claim 1 has been canceled.

Claims 2 and 8 have been amended as follows.

2. (Amended) [The method of claim 1] A method of fabricating a semiconductor device, comprising:

forming a conductive region at the top of a semiconductor substrate;

forming a first interlayer dielectric layer on the semiconductor substrate over the entirety of the conductive region;

forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer;

forming a second interlayer dielectric layer on the conductive line;

removing portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer which overlie the conductive region to form a contact hole which exposes the conductive region; and

filling the contact hole with a conductive material to connect the conductive line to the conductive region,

wherein said removing of portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer comprises:

forming a patterned photosensitive film on the second interlayer dielectric layer, the patterned photosensitive film defining an opening therein having a width that is greater than [the critical dimension] a width of the conductive line,

etching the second interlayer dielectric layer using the photosensitive film pattern as an etch mask until the conductive line is exposed, and

etching the conductive line and the first interlayer dielectric layer using the etched second interlayer dielectric layer as an etch mask.

8. (Amended) [The method of claim 1] A method of fabricating a semiconductor device, comprising:

forming a conductive region at the top of a semiconductor substrate;

forming a first interlayer dielectric layer on the semiconductor substrate over the entirety of the conductive region;

forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer;

forming a second interlayer dielectric layer on the conductive line;

removing portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer which overlie the conductive region to form a contact hole which exposes the conductive region; and

filling the contact hole with a conductive material to connect the conductive line to the conductive region,

wherein the forming of the conductive line comprises:

forming a dielectric film pattern defining a line-shaped opening on the first interlayer dielectric layer, and

depositing conductive material in the line-shaped opening.